Computer Organization and Assembly Language

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Instruction Cycle

- Two steps:
  - Fetch
  - Execute
Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches instruction from memory location pointed to by PC
- Increment PC
  - Unless told otherwise
- Instruction loaded into Instruction Register (IR)
- Processor interprets instruction and performs required actions
Execute Cycle

- Processor-memory
  - data transfer between CPU and main memory
- Processor I/O
  - Data transfer between CPU and I/O module
- Data processing
  - Some arithmetic or logical operation on data
- Control
  - Alteration of sequence of operations
    - e.g. jump
- Combination of above
CPU Connection

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts
Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
What is a Bus?

- A communication pathway connecting two or more devices
- Usually broadcast
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown
Data Bus

• Carries data
  — Remember that there is no difference between “data” and “instruction” at this level

• Width is a key determinant of performance
  — 8, 16, 32, 64 bit
Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space
Control Bus

- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals
Bus Interconnection Scheme

- CPU
- Memory
- Memory
- I/O
- I/O

Control Lines
Address Lines
Data Lines

Bus
What do buses look like?
- Parallel lines on circuit boards
- Ribbon cables
- Strip connectors on mother boards
  - e.g. PCI
- Sets of wires
Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems
High Performance Bus

Processor -> Local Bus -> Cache/Bridge -> System Bus

Main Memory

SCSI -> P1394 -> Graphic -> Video -> LAN

High-Speed Bus

FAX

Expansion bus interface

Modem

Serial

Expansion Bus
Bus Types

- Dedicated
  - Separate data & address lines

- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance